

Application No.: 10/065,212

Amendment dated February 07, 2005

Amendment made in response to Office Action dated November 10, 2004

Amendments to the Claims

This listing of claims will replace all prior versions and listing of claims in the application:

Listing of Claims:

1. (currently amended) An IC comprising:

a memory cell array having a plurality of memory cells, wherein the memory cells includes at least first and second ports forming a memory cell array with at least first and second access ports for accessing the memory cells;

~~a first and a second port, each of said memory cells being coupled to said first and second ports;~~

a cache memory coupled ~~being connected~~ to said first and second access ports, wherein during a read operation to the memory cell array to obtain read data ~~subject to one of said memory cells~~ through one of said first and second access ports, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory ~~a data stored in said one of said memory cells is read out from said cache memory if it is determined that said cache memory contains said data stored in said one of said memory cells;~~ and

a refresh control circuit for performing refresh operations ~~efresh of the information stored within said memory cells, said refresh control circuit refreshing memory cells through one of said ports while reading data out of said cache memory.~~

2. (original) The IC according to claim 1, wherein said cache memory comprises a tag portion, an address portion, and a data portion corresponding to each other, wherein said

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tag portion indicates if said corresponding address and data portions contain valid address and data values.

3. (currently amended) The IC according to claim 2, wherein said first and second access ports each comprises an address path and a data read path, said address paths of said first and second ports being connected to said address portion of said cache memory and said data read paths of said first and second ports being connected to said data portion.
4. (currently amended) The IC according to claim 3, wherein said cache memory comprises an address comparator which is coupled to said address path of at least one of said first and second access ports.
5. (currently amended) The IC according to claim 4, wherein said address comparator ~~is designed to compare~~ compares an address being provided through said at least one of said access ports and an address being provided from said address portion of said address memory, and in case of a match designed to output the data stored in the corresponding memory cell onto the read path of said at least one port.
6. (currently amended) The IC according to claim 5, wherein in case of said match of addresses a refresh for a row of memory cells within the memory cell array is performed through the second access port.
7. (currently amended) The IC according to claim 6, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a

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second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

8. (original) The IC according to claim 7, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.

9. (currently amended) The IC according to claim 5, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

10. (original) The IC according to claim 9, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.

11. (currently amended) The IC according to claim 1, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

12. (original) The IC according to claim 11, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said

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first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.

13. (currently amended) An IC comprising:

a memory cell array having a plurality of dynamic

memory cells, wherein the memory cells comprise at least first and second ports to form a memory array having at least first and second access ports accessing the memory cells;

~~a first port and a second port for performing an access to at least one of said memory cells;~~

a refresh control circuit to perform a refresh for said memory cells once within a retention time interval;

a cache memory connected to at least one of said ports;

a switching device coupled to said at least one of said ports, said cache memory, and said memory cell array; and

said switching device being operated to connect either one of said memory cell array and said cache memory to said at least one of said access ports in response to a read operation.

14. (currently amended) The IC according to claim 13, wherein said refresh control circuit performs a refresh operation while a read operation is performed through said at least one of said access ports from said cache memory.

15. (original) The IC according to claim 13, wherein said cache memory comprises a tag portion, an address portion, and a data portion corresponding to each other, wherein said tag portion indicates if said address and data portions contain valid address and data values.

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16. (currently amended) The IC according to claim 13, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

17. (currently amended) A IC comprising:
a memory cell array having a plurality of memory cells with at least first and second ports forming a memory cell array with at least first and second access ports;
~~a first and a second port coupled to each one of said memory cells;~~
a cache memory coupled to said first and second ports;
said first and second access ports comprising address terminals and data terminals; and
said second access port being controlled by a refresh control circuit to perform a refresh of said memory cells.

18. (currently amended) The IC according to claim 17, wherein a refresh operation is performed for a row of memory cells through said second access port, and a read command received through said second access port is performed through said cache memory in parallel to said refresh operation.

19. (currently amended) The IC according to claim 17, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first access port and a second selection transistor coupled to said second access port and a storage node connected to said first and second selection transistors.

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20. (new) An IC comprising:

a memory cell array having a plurality of memory cells, wherein the memory cells includes at least first and second ports forming a memory cell array with at least first and second access ports, wherein at least one of the first and second ports are used for memory accesses; and

a cache memory coupled to at least the access ports used for memory, the cache memory provides the read data if the read data is contained therein or the memory cell array provides the read data if the read data is not contained in the cache memory.

21. (new) The IC according to claim 21 wherein the at least one of the first and second access ports used for memory accesses comprises an address path and a data read path, said address path connected to said address portion of said cache memory and said data read path of the at least one of the first and second access ports for memory accesses is connected to said data portion.

22. (new) The IC according to claim 21 comprises a refresh control circuit for performing refresh operations through the other of the first and second access ports.

23. (new) The IC according to claim 20 wherein the at least first and second access ports are used for memory accesses.

24. (new) The IC according to claim 23 wherein said first and second access ports each comprises an address path and a data read path, said address paths of said first and second ports being connected to said address portion of said cache memory and said data read paths of said first and second ports being connected to said data portion.

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25. (new) The IC of claim 24 comprises a refresh control circuit for performing refresh operations through either one of the access ports